We Claim:

1. In an information processing system, having a plurality of modules including a processor, a main memory and a plurality of I/O devices, a data transfer switch for performing data transfer operations between said processor, main memory and I/O devices comprises:

a request bus having a request bus arbiter for receiving read and write requests from each one of said plurality of modules;

a processor memory bus configured to receive address and data information from a predetermined number of said modules including said processor, said processor memory bus having a data bus arbiter for receiving data read and write requests from each one of said predetermined number of modules coupled to said processor memory bus;

an internal memory bus configured to receive address and data information from a predetermined number of said modules including said memory and said I/O devices, said internal memory bus having a data bus arbiter for receiving data read and write requests from each one of said predetermined number of modules coupled to said internal memory bus; and

a transceiver system coupled to said processor memory bus and said internal memory bus for transferring data between said processor memory bus and said internal memory bus.

2. A data transfer switch in accordance with claim 1 wherein said request bus arbiter is configured to receive a plurality of read and write requests each having a specifiable

priority level, wherein said requests are served in a descending order of priority.

3. A data bus transfer switch in accordance with claim 2, wherein said request bus further comprises signal lines for receiving a destination address and a requestor's identification information.

4. A data bus transfer switch in accordance with claim 2, wherein each one of said modules configured to provide information in request to a requesting module provides a transaction identification signal to said requesting module.

5. A data transfer switch in accordance with claim 4 wherein said request bus includes signal lines for receiving from each one of said modules, the types of commands to be processed.

6. A data transfer switch in accordance with claim 5 wherein said commands include a memory operation and a programmable input/output operation corresponding to data transfer operations between memory modules and between input/output device modules and remaining modules of the system.

7. A data transfer switch in accordance with claim 6 wherein in response to a requesting module to conduct one of said commands, a responding module sends a ready signal.

8. A data transfer switch in accordance with claim 7, wherein said responding module provides an update signal to said request bus arbiter so as to indicate whether additional commands can be handled.

9. A data transfer switch in accordance with claim 8, wherein said module providing a request command to said request bus, provides a data request operation to one of said internal memory bus and processor memory bus..

10. A data transfer switch in accordance with claim 6, wherein said requesting module provides a write request, a responding module identification signal and a priority signal to one of said internal memory bus arbiter and processor memory bus arbiter.

11. A data transfer switch in accordance with claim 6, wherein a requesting module to request bus arbiter becomes a data master when it is ready to respond and provide requested data.

12. A data transfer switch in accordance with claim 1 further comprising a second set of connection lines from at least one of said modules to said request bus arbiter to allow back-to-back requests.

13. A data transfer switch in accordance with claim 12, wherein a module after asserting a first request to said request bus arbiter asserts a second request while waiting for said

first request be granted.

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14. In an information processing system, having a plurality of modules including a processor, a cache memory, a main memory and a plurality of I/O devices, a data streamer for performing data transfer operations between said modules comprises:

a channel state memory configured to store a first allocated channel information corresponding to a data transfer operation from a source module to said data streamer, and further configured to store a second allocated channel information corresponding to said data transfer operation from said data streamer to a destination module; and

a buffer memory allocated to said data transfer operation for receiving data provided by said source module in accordance with said first allocated channel information and providing said received data to said destination module in accordance with said second allocated channel information.

15. The data streamer in accordance with claim 14 wherein said channel state memory stores information corresponding to a plurality of data transfer operations between said modules.

16. The data streamer in accordance with claim 14, wherein a buffer memory is allocated for each one of said data transfer operations and the size of said buffer memory variably changes in accordance with the size of data in a corresponding data transfer operation.

17. The data streamer in accordance with claim 16 wherein the data transfer rate from a source module to a corresponding buffer in said buffer memory, is different than the data transfer rate from said buffer memory to a destination module.

18. The data streamer in accordance with claim 17 wherein said first allocated channel information includes a first channel descriptor, wherein said data transfer operation from a source module to said buffer is accomplished in accordance with said first channel descriptor.

19. The data streamer in accordance with claim 18, wherein said second allocated channel information includes a second channel descriptor, wherein said data transfer operation from said buffer to said destination module is accomplished in accordance with said second channel descriptor.

20. The data streamer in accordance with claim 19, wherein said first and said second channel descriptors have a different format.

21. The data streamer in accordance with claim 14 wherein said data transfer operation from a source module to a destination module includes a data cache operation having a coherent allocation policy.

22. The data streamer in accordance with claim 14 wherein said data transfer operation from a source module to a destination module includes a data cache operation having a

coherent no-allocation policy.

23. The data streamer in accordance with claim 14 wherein said data transfer operation from a source module to a destination module includes a data cache operation having a non-coherent no-allocation policy.

24. In an information processing system, having a plurality of modules including a processor, a cache memory, a main memory and a plurality of I/O devices, a data streamer for performing data transfer operations between said modules comprises:

a channel state memory configured to store a plurality of allocated channel information defining a plurality of source channels each of which corresponding to a data transfer operation from a source module to said data streamer, and further configured to store a plurality of allocated channel information defining a plurality of destination channels each of which corresponding to said data transfer operation from said data streamer to a destination module;

a buffer memory allocated to said data transfer operation for receiving data provided by said source module in accordance with said first allocated channel information and providing said received data to said destination module in accordance with said second allocated channel information; and

a transfer engine coupled to said channel state memory and configured to service a plurality of data paths, on a preassigned priority order, wherein each data path is defined by at least one channel having corresponding information stored in said channel state memory,

said data path also defined by said buffer memory corresponding to said channel

25. The data streamer in accordance with claim 24, wherein a predetermined buffer space within said buffer memory is allocated for each one of said data transfer operations and the size of said buffer space variably changes in accordance with the size of data in a corresponding data transfer operation.

26. The data streamer in accordance with claim 25 wherein the data transfer rate from a source module to a corresponding buffer space in said buffer memory, is different than the data transfer rate from said buffer space to a destination module.

27. The data streamer in accordance with claim 26 wherein each of said source channels includes a first channel descriptor, wherein said data transfer operation from a source module to said buffer is accomplished in accordance with said first channel descriptor.

28. The data streamer in accordance with claim 26, wherein said destination channel includes a second channel descriptor, wherein said data transfer operation from said buffer space to said destination module is accomplished in accordance with said second channel descriptor.

29. The data streamer in accordance with claim 28, wherein said first and said second channel descriptors have a different format.

30. The data streamer in accordance with claim 29 wherein said data transfer operation from a source module to a destination module includes a data cache operation having a coherent allocation policy.

31. The data streamer in accordance with claim 29 wherein said data transfer operation from a source module to a destination module includes a data cache operation having a coherent no-allocation policy.

32. The data streamer in accordance with claim 29 wherein said data transfer operation from a source module to a destination module includes a data cache operation having a non-coherent no-allocation policy.

33. In an information processing system, having a plurality of modules including a processor, a cache memory, a main memory and a plurality of I/O devices, a method for performing data transfer operations between said modules comprising the steps of:

storing a first allocated channel information corresponding to a data transfer operation from a source module to a buffer memory;

storing a second allocated channel information corresponding to said data transfer operation from said buffer memory to a destination module;

receiving data provided by said source module in accordance with said first allocated channel information; and

providing said received data to said destination module in accordance with

said second allocated channel information.

34. The method in accordance with claim 33 further comprising the step of storing a plurality of said channel information each of which corresponding to a data transfer operation.

35. The method in accordance with claim 34, further comprising the step of allocating a buffer memory space within said buffer memory, and changing the size of said buffer memory space in accordance with the size of data in a corresponding data transfer operation.

36. The method in accordance with claim 35 further comprising the step of setting the data transfer rate from a source module to a corresponding buffer memory space at a different rate than the data transfer rate from said buffer memory space to a destination module.

37. The method in accordance with claim 36, further comprising the step of transferring data in accordance with a predetermined channel descriptor.

38. The method in accordance with claim 37 data streamer in accordance with claim 14 wherein said data transfer operation from a source module to a destination module includes a data cache operation having a coherent allocation policy.

39. The data streamer in accordance with claim 33 further comprising the step

of providing data transfers having a data cache operation with a coherent no-allocation policy.

40. The data streamer in accordance with claim 33 further comprising the step of providing data transfers having a data cache operation with a non-coherent no-allocation policy.